CLAIMS

1. A method of reducing a rate for refreshing a portion of a dynamic random access memory (DRAM), comprising:

storing information for distinguishing between a first portion of a DRAM requiring refresh at a first rate and a second portion of said DRAM permitting refresh at a second rate lower than said first rate; and

accessing said stored information to refresh said first portion at said first rate and to refresh said second portion at said second rate.

2. A method as claimed in claim 1 wherein said first portion and said second portion each include one or more segments of said DRAM, and said information allows said first portion and said second portion to be distinguished on the basis of said segments.

3. A method as claimed in claim 1 wherein said first portion includes subportions, at least some of said subportions being physically discontiguous.

4. A method as claimed in claim 3 wherein said subportions are wordline spaces of said DRAM and said information allows said first portion and said second portion to be distinguished on the basis of said wordline spaces.

5. A method as claimed in claim 1 wherein said first portion is refreshed at said first rate and said second portion is refreshed at said second rate while both said first portion and said second portion operate in a mode selected from the group consisting of active mode and sleep mode.

6. A method as claimed in claim 1 wherein said information is stored in said DRAM.

7. A method as claimed in claim 6 wherein said information is further stored in a non-volatile memory and accessed from said non-volatile memory for storage in said DRAM.

8. A method as claimed in claim 6 wherein said information is stored on one or more fuses on an integrated circuit including said DRAM.

9. A method as claimed in claim 1 wherein said information further allows a plurality of portions numbering one to *n* of said DRAM including said first portion and said second portion to be distinguished for refreshing said plurality of portions of said DRAM at a plurality of respective rates numbering one to *n*, and said stored information is accessed to refresh said plurality of portions at said respective rates including to refresh said first portion at said first rate, to refresh said second portion at said second rate, and to refresh said *n*th portion at said *n*th rate.

10. A method as claimed in claim 6 wherein said information is stored in a space accessible through one or more wordlines of said DRAM.

11. A method as claimed in claim 1 wherein said information is generated by post-fabrication stress testing of said DRAM.

12. An integrated circuit including a dynamic random access memory (DRAM), comprising:

a first portion requiring refresh at a first rate and a second portion permitting refresh at a second rate lower than said first rate; and

electronic means operable to store information for distinguishing between said first portion and said second portion; and

a controller operable to access said stored information from said electronic means to refresh said first portion at said first rate and to refresh said second portion at said second rate.

13. An integrated circuit as claimed in claim 12 wherein said first portion and said second portion each include one or more segments of said DRAM, and said information allows said first portion and said second portion to be distinguished on the basis of said segments.

14. An integrated circuit as claimed in claim 12 wherein said first portion includes subportions, at least some of said subportions being physically discontiguous.

15. An integrated circuit as claimed in claim 14 wherein said subportions are wordline spaces of said DRAM such that said information allows said first portion and said second portion to be distinguished on the basis of said wordline spaces.

16. An integrated circuit as claimed in claim 12 wherein said controller is operable to refresh said first portion at said first rate and to refresh said second portion at said second rate while both said first portion and said second portion operate in a mode selected from the group consisting of active mode and sleep mode.

17. An integrated circuit as claimed in claim 12 wherein said electronic means is located within said DRAM.

18. An integrated circuit as claimed in claim 17 wherein said controller is further operable to access first information from a non-volatile memory and said electronic means is further operable to store said information from said first information.

19. An integrated circuit as claimed in claim 18 wherein said electronic means includes one or more fuses.

20. An integrated circuit as claimed in claim 12 wherein said information further allows a plurality of portions numbering one to *n* of said DRAM including said first portion and said second portion to be distinguished for refreshing said plurality of portions of said DRAM at a plurality of respective rates numbering one to *n*, and said controller is operable to refresh said plurality of portions at said respective rates including to refresh said first portion at said first rate, to refresh said second portion at said second rate, and to refresh said *n*th portion at said *n*th rate.

21. An integrated circuit as claimed in claim 20 wherein said electronic means includes a space accessible through one or more wordlines of said DRAM.